SAT 101: Solving Challenging Optimization Problems using Advanced Boolean Satisfiability and ILP Techniques

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Abstract
Recent years have seen a tremendous growth in the number of research and development groups at universities, research labs, and companies that have started using Boolean Satisfiability (SAT) algorithms for solving different decision and optimization problems in Computer Science and Engineering. This has lead to the development of highly-efficient SAT solvers that have been successfully applied to solve a wide-range of problems in Electronic Design Automation (EDA), Artificial Intelligence (AI), Networking, Fault Tolerance, Security, and Scheduling. Examples of such problems include automatic test pattern generation for stuck-at faults (ATPG), formal verification of hardware and software, circuit delay computation, FPGA routing, power leakage minimization, power estimation, circuit placement, graph coloring, wireless communications, wavelength assignment, university classroom scheduling, and failure diagnosis in wireless sensor networks.

SAT solvers have recently been extended to handle Pseudo-Boolean (PB) constraints which are linear inequalities with integer coefficients. This feature allowed SAT solvers to handle optimization problems, as opposed to only decision problems, and to be applied to a variety of new applications. Recent work has also showed that free open source SAT-based PB solvers can compete with the best generic Integer Linear Programming (ILP) commercial solvers such as CPLEX.

This tutorial is aimed at introducing the latest advances in SAT technology. Specifically, we describe the simple new input format of SAT solvers and the common SAT algorithms used to solve decision/optimization problems. In addition, we highlight the use of SAT algorithms in solving a variety of EDA decision and optimization problems and compare its performance to generic ILP solvers. This should guide researchers in solving their existing decision and optimization problems using the new SAT technology. We discuss how to detect and break symmetries in SAT instances and the effect of that in significantly speeding up the search process. Finally, we provide a prospective on future work on SAT.

Area of Tutorial / Keywords
Electronic Design Automation (EDA), Search, Optimization, Boolean Satisfiability, Integer Linear Programming (ILP), Structure & Symmetry. Applications (Testing, Verification, Routing, Placement, Power Optimization, Circuit Delay Computation, etc.).

Expected Background of Participants
Students (undergraduate and graduate), engineers, researchers, and faculty in Computer Science and Engineering.

Tutorial Format
The tutorial can be delivered over a 1/2 day period.

Learning Outcomes and Benefits
1. Attendees will learn about the latest advances in SAT/ILP technology, including the simple SAT input format, how SAT solvers work, what advances have been proposed to speed up the search process.
2. Attendees will learn how SAT algorithms are used in solving a variety of challenging Engineering decision and optimization problems. This should guide researchers in solving their existing decision and optimization problems using the new SAT/ILP technology.
3. Attendees will learn about some advanced SAT algorithms, including how to detect and break symmetries in SAT instances and the effect of that in significantly speeding up the search process.
4. Attendees will learn about the future work on SAT.

Tentative Outline of the Tutorial

2. Describe the input format of SAT solvers (including the new Pseudo Boolean PB constraints)
3. Survey of the main algorithms used in SAT solvers. This includes:
   - Local search
   - Backtrack search
   - Algebraic manipulation
4. In-depth analysis of backtrack search, the most commonly used SAT solving strategy. This includes:
   - Intelligent decision heuristics
   - Identification of necessary assignments
   - Non-chronological backtracking
   - Clause recording
   - Randomization and restarts
5. Survey of the well-known decision and optimization applications of SAT in Electronic Design Automation (EDA), Networking, Scheduling, and Artificial Intelligence (AI). Specifically:
   - Formal verification of software and hardware
   - Power leakage minimization
   - Circuit delay computation
   - FPGA routing
   - Graph coloring
   - University classroom scheduling
   - Routing in optical networks
   - Fault tolerance in wireless sensor networks
6. Describe the recent utilization of SAT technology to solve linear optimization, i.e. 0-1 ILP, problems. Provide an overview of the latest 0-1 ILP SAT solvers.
7. Compare the performance of SAT-based 0-1 ILP solvers to generic-based ILP solvers, e.g. CPLEX.
8. Explain how pre-processing tools, based on detecting symmetries and sparsity in ILP instances, work and how they can significantly speed up the search process. Provide real examples using existing tools.
9. Provide a perspective on future work on SAT and ILP by highlighting the techniques and applications that show promise in the near future.

Instructor Qualifications

Fadi Aloul is an Associate Professor of Computer Engineering at the American University of Sharjah, UAE. He holds a Ph.D. and M.S. degrees in Computer Science & Engineering from the University of Michigan, Ann Arbor, USA, respectively, and a B.S. degree in Electrical Engineering summa cum laude from Lawrence Technological University (LTU), Michigan, USA. His areas of expertise include electronic design automation, optimization and computer security. He is a Certified Information Systems Security Professional (CISSP).

Dr. Aloul received a number of awards including the prestigious H.H. Sheikh Khalifa, UAE's President, Award for Higher Education, the Abdul Hameed Shoman Award for Young Arab Researchers, the AUS Excellence in Teaching Award and the Semiconductor Research Corporation (SRC) Research Fellowship. He has 95+ publications and 1 US patent. He developed several tools used in the SAT domain, such as the award-winning 0-1 ILP SAT solver and optimizer, PBS. He is a regular invited speaker and panelist across a number of international conferences related to Technology, Cyber-Security and Education. He is a senior member of the Institute of Electrical and Electronics Engineers (IEEE) and the Associate of Computing Machinery (ACM). He is the founder and chair of the UAE IEEE Graduates of Last Decade (GOLD) group, an organization dedicated to advancing technological innovation and excellence for the benefit of humanity. Additional information can be found at http://www.aloul.net.